REMARKS

By this Amendment, claims 2-4 are cancelled, claims 1 and 5-6 are amended, and claims 7-20 are added. Thus, claims 1 and 5-20 are active in the application. Reexamination and reconsideration of the application are respectfully requested.

The specification and abstract have been carefully reviewed and revised in order to correct grammatical and idiomatic errors in order to aid the Examiner in further consideration of the application. The amendments to the specification and abstract are incorporated in the attached substitute specification and abstract. <u>No new matter has been added</u>.

Also attached hereto is a marked-up version of the substitute specification and abstract illustrating the changes made to the original specification and abstract.

On page 2 of the Office Action, claims 1-6 were rejected under 35 U.S.C. § 102(b) as being anticipated by Motoyama et al. (U.S. 6,099,992). This rejection is believed to be moot with respect to claims 2-4 in view of the cancellation of these claims.

Without intending to acquiesce to this rejection, independent claim 1 has been amended in order to more clearly illustrate the marked differences between the present invention and the applied reference. Accordingly, the Applicant submits that claim 1 is patentable for the following reasons. Furthermore, the Applicants submit that this rejection is inapplicable to new claims 7-20 for the following reasons.

The present invention provides a semiconductor device having dummy patterns. The dummy patterns of the present invention are formed in standard areas, as shown in Figures 1(A), 3(A), 4(A) and 5(A). In each of the standard areas, a plurality of dummy line patterns (Figure 1(A)) or a singe pattern with an opening (Figures 3(A), 4(A), 5(A)) are formed. Accordingly, since each of the standard areas has a space portion, i.e., a space between the line patterns or the opening, a pattern ratio of the semiconductor device is reduced. Therefore, as described, for example, in lines 5-9 on page 10 of the original specification, an advantageous effect of the present invention is that it is possible to more effectively suppress an increase in the global step.

Independent claims 1, 9 and 14 each recite the semiconductor device of the present invention as having the above-described features.

Claim 1 recites a semiconductor device which comprises a semiconductor substrate having a pattern forming region and a pattern non-forming region, and a wiring pattern formed on the pattern forming region. The semiconductor device of claim 1 also comprises a plurality of dummy patterns formed on the pattern non-forming region, where the plurality of dummy patters are formed within a plurality of standard areas, and an insulating film formed on the wiring pattern and the plurality of dummy patterns. As defined in claim 1, each of the plurality dummy patterns is spaced apart with a width filled by plus sizing of the insulating film formed on the plurality of dummy patterns.

New claim 9 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, and a conductive pattern formed on the pattern area of the semiconductor substrate. The semiconductor device of new claim 9 also comprises a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate, where each of the plurality of dummy patterns has a standard rectangular outline and is arranged in a matrix with predetermined spacing. As defined in new claim 9, each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced.

New claim 14 recites a semiconductor device which comprises a semiconductor substrate having a pattern area and a non-pattern area, a conductor pattern formed on the pattern area of the semiconductor substrate, and a plurality of dummy patterns formed on the non-pattern area of the semiconductor substrate. As defined in new claim 14, each of the plurality of dummy patterns are formed in a plurality of standard areas being arranged in a matrix with predetermined spacing, and each of the plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of the semiconductor device is reduced.

Motayama et al. discloses a semiconductor device in which interconnection patterns 21 are laid on a substrate, and first dummy patterns 22 are disposed at a fixed interval W from the interconnection patterns 21 (see Column 7, lines 26-29 and Figure 5A). A lattice-like pattern 23 is then laid onto the first dummy patterns 22, and the portions of the first dummy patterns which are disposed under the lattice-like (reticular) pattern 23 are removed to form second (divided and separated) dummy patterns 22d-22h (see Column 7, lines 30-39 and Figures 5B-5C).

Motyama et al. also discloses that the widths of the second dummy patterns 22d-22h are measured to find whether or not any of the widths thereof fall short of the smallest allowable width, a. If any of the second dummy patterns 22d-22h are determined to have a width smaller than the smallest allowable width (i.e., dummy patterns 22e-22f in Figure 5C), a third dummy pattern 22i which was removed as being disposed under the lattice-like pattern 23 are restored by being adjoined to the dummy patterns 22e-22f so as to ensure that each of the restored second dummy patterns 22e-22f have a width equal to or larger than the smallest allowable width (see Column 7, lines 47-67 and Figures 5C-5D).

Motoyama et al. discloses that after the widths of the second dummy patterns 22d-22h are determined and restored if smaller than the smallest allowable width, the areas of the second dummy patterns 22d, 22g, 22h are measured to determine if whether or not any of the second dummy patterns has an area which is smaller than the smallest allowable area, S. If any of the second dummy patterns has an area smaller than the smallest allowable area, the third dummy pattern 221 which was removed as being disposed under the lattice-like pattern 23 are restored by being adjoined to the second dummy patterns having the smaller than allowable area in a manner similar to the process of restoring the second dummy patterns 22e-22f to have an allowable width (see Column 8, lines 1-27 and Figures 5D-5E).

Accordingly, Motayama et al. discloses a semiconductor device having dummy patterns. Motayama et al. also discloses that all of the areas including pattern areas and non-pattern areas are divided into standard areas by using the lattice-like pattern 23, as shown in Figure 5B.

However, Motayama et al. clearly does not disclose or suggest that a single dummy pattern or a plurality of dummy patterns with an opening is/are formed in each of the standard areas. That is, as shown, for example, by arrow 1.65 in Figure 7A, a <u>single dummy pattern without an opening or space portion</u> is formed in each standard area, and there is only a single dummy pattern in each standard area.

Accordingly, Motayama et al. clearly does not disclose or suggest that <u>each of the plurality dummy patterns is spaced apart with a width</u> filled by plus sizing of the insulating film formed on the plurality of dummy patterns, as recited in claim 1.

Similarly, Motayama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has an opening so that a pattern ratio of the semiconductor device is reduced, as recited in new claim 9. Moreover, Motayama et al. clearly does not disclose or suggest that each of the plurality of dummy patterns has a space portion within each of the standard areas so that a pattern ratio of the semiconductor device is reduced, as recited in new claim 14.

Accordingly, Motayama et al. clearly does not disclose or suggest each and every limitation of claims 1, 9 and 14.

Therefore, claims 1, 9 and 14 are clearly not anticipated by Motayama et al. since Motayama et al. fails to disclose each and every limitation of claims 1, 9 and 14. Accordingly, it is submitted that the claims 1, 9 and 14, as well as claims 5-8, 10-13 and 15-20 which depend therefrom, are clearly allowable over the prior art as applied by the Examiner.

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. An early notice thereof is respectfully solicited.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

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